Similar to Bipolar Junction Transistor. JFET can also be used as an amplifier. The ac equivalent circuit of a JFET is shown in **fig. 1.**

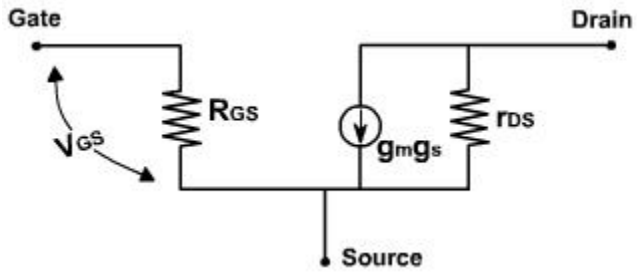

Fig. 1

The resistance between the gate and the source R_{GS} is very high. The drain of a JFET acts like a current source with a value of $g_m V_{gs}$. This model is applicable at low frequencies.
From the ac equivalent model

$$i_d = g_m V_{gs} + \frac{V_{ds}}{r_d}$$

$$\text{When } i_d = 0, \quad \frac{V_{ds}}{V_{gs}} = -g_m r_d$$

The amplification factor μ for FET is defined as

$$\mu = \left.\frac{v_{ds}}{v_{gs}}\right|_{i_d=0} \qquad \therefore \mu = g_m r_d$$

When $V_{GS} = 0$, g_m has its maximum value. The maximum value is designated as $g_{mo.}$
Again consider the equation,

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]\left[\frac{-1}{V_{GS(off)}}\right]$$

$$g_m = \frac{-2I_{DSS}}{V_{GS(Off)}}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]$$

$$\text{When } \quad V_{GS} = 0, \; g_m = g_{mo} = \frac{-2I_{DSS}}{V_{GS(off)}}$$

$$\therefore g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]$$

As V_{GS} increases, gm decreases linearly.

$$V_{GS(off)} = \frac{-2I_{DSS}}{g_{mo}}$$

Measuring I_{DSS} and g_m, $V_{GS(off)}$ can be determined

FET as Amplifier:

Fig. 2, shows a common source amplifier.

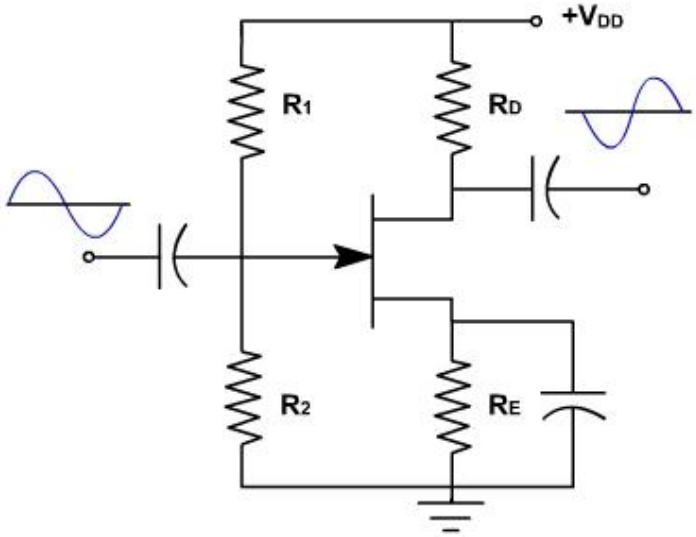

Fig. 2

When a small ac signal is coupled into the gate it produces variations in gate source voltage. This produces a sinusoidal drain current. Since, an ac current flows through the drain resistor. An amplified ac voltage is obtained at the output. An increase in gate source voltage produces more drain current, which means that the drain voltage is decreasing. Since the positive half cycle of input voltage produces the negative half cycle of output voltage, we get phase inversion in a CS amplifier.

The ac equivalent circuit is shown in **fig. 3.**

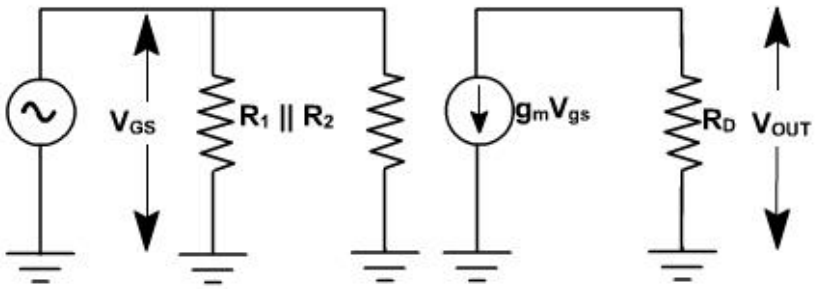

Fig. 3

The ac output voltage is

$v_{out} = - g_m v_{gS} R_D$

Negative sign means phase inversion. Because the ac source is directly connected between the gate source terminals therefore ac input voltage equals

$V_{in} = V_{gs}$

The voltage gain is given by

$$A_V = \frac{v_{out}}{v_{in}} = - g_m R_D$$

$A_V =$ unloaded voltage gain

The further simplified model of the amplifier is shown in fig. 4.

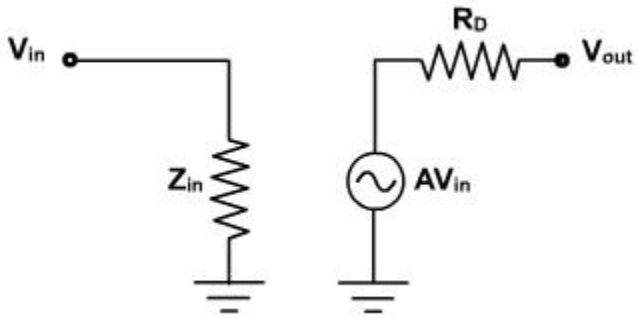

Fig. 4

Z_{in} is the input impedance. At low frequencies, this is parallel combination of R_1|| R_2|| R_{GS}. Since R_{GS} is very large, it is parallel combination of R_1 & R_2. A V_{in} is output voltage and R_D is the output impedance. Because of nonlinear transconductance curve, a JFET distorts large signals, as shown in fig. 5.

Given a sinusoidal input voltage, we get a non-sinusoidal output current in which positive half cycle is elongated and negative cycle is compressed. This type of distortion is called Square law distortion because the transconductance curve is parabolic.

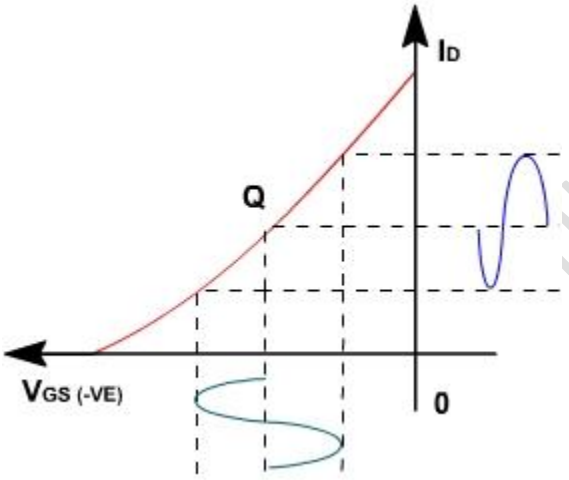

Fig. 5

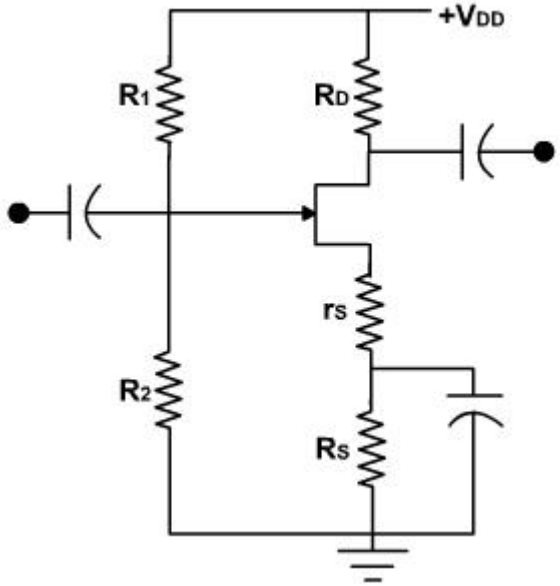

Fig. 6

This distortion is undesirable for an amplifier. One way to minimize this is to keep the signal small. In that case a part of the curve is used and operation is approximately linear. Sometimes swamping resistor is used to minimize distortion and gain constant. Now the source is no longer ac ground as shown in fig.6. The drain current through r_S produces an ac voltage between the source and ground. If r_S is large enough the local feedback can swamp out the non-linearity of the curve. Then the voltage gain approaches an ideal value of R_D / r_S.

Since R_{GS} approaches infinity therefore, all the drain current flows through r_S producing a voltage drop of g_m V_{gS} r_S. The ac equivalent circuit is shown in **fig. 7.**

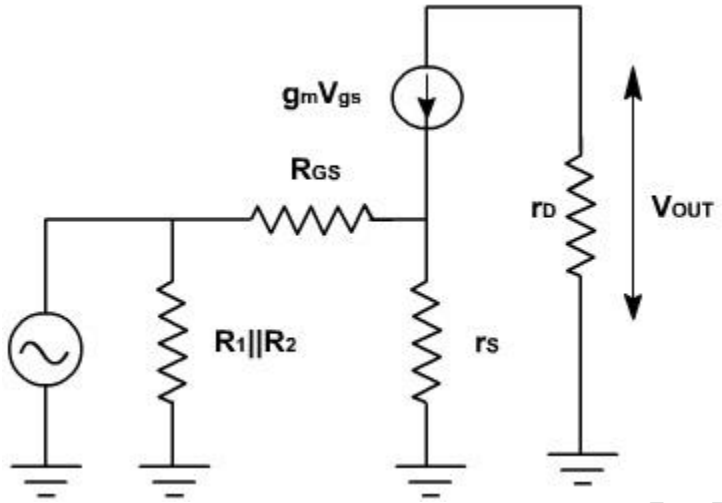

Fig. 7

$$v_{gs} + g_m\ v_{gs}\ r_s - v_{in} = 0$$

$$v_{in} = (1 + g_m r_s)\ v_{gs}$$

$$v_{out} = -g_m R_D\ v_{gs}$$

$$A = \frac{-g_m R_D}{1 + g_m r_s} = \frac{-R_D}{r_s + 1/g_m}$$

The voltage gain reduces but voltage gain is less effective by change in g_m. r_S must be greater than $1 / g_m$ only then

$$v_{gs} = -\frac{R_D}{r_s}$$

Design of JFET amplifier:

To design a JFET amplifier, the Q point for the dc bias current can be determined graphically. The dc bias current at the Q point should lie between 30% and 70% of I_{DSS}. This locates the Q point in the linear region of the characteristic curves.

The relationship between i_D and v_{GS} can be plotted on a dimensionless graph (i.e., a normalized curve) as shown in **fig. 8.**

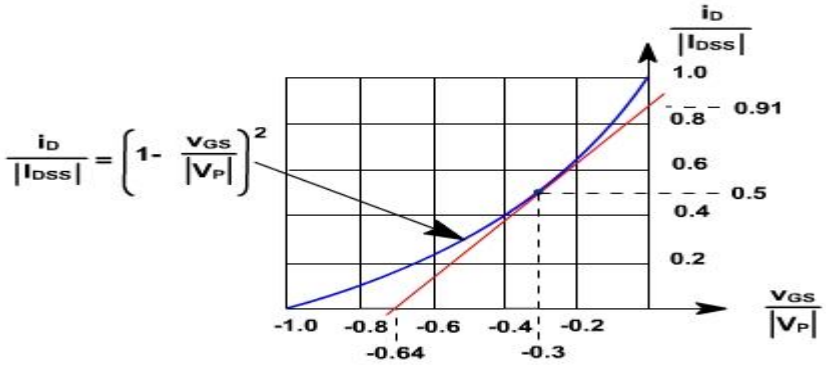

Fig. 8

The vertical axis of this graph is i_D / I_{DSS} and the horizontal axis is v_{GS} / V_P. The slope of the curve is g_m.

A reasonable procedure for locating the quiescent point near the center of the linear operating region is to select $I_{DQ} \approx I_{DSS} / 2$ and $V_{GSQ} \approx 0.3V_P$. Note that this is near the midpoint of the curve. Next we select $v_{DS} \approx V_{DD} / 2$. This gives a wide range of values for v_{ds} that keep the transistor in the pinch off mode.
The transconductance at the Q-point can be found from the slope of the curve of **fig.8** and is given by

$$g_m = \frac{1.41\ I_{DSS}}{V_P}$$