LECTURE NOTES
Field Effect Transistor

Branch: Electronics

Semester: Second

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Field Effect Transistor

Field effect Transistor is a semiconductor device which depends for its operation on the control of current by an electric Field

Field Effect Transistor

FET has several advantages over BJT

1. Current flow is due to majority carriers only
2. Immune to radiation
3. High input resistance
4. Less noisy than BJT
5. No offset voltages at zero drain current
6. High thermal stability

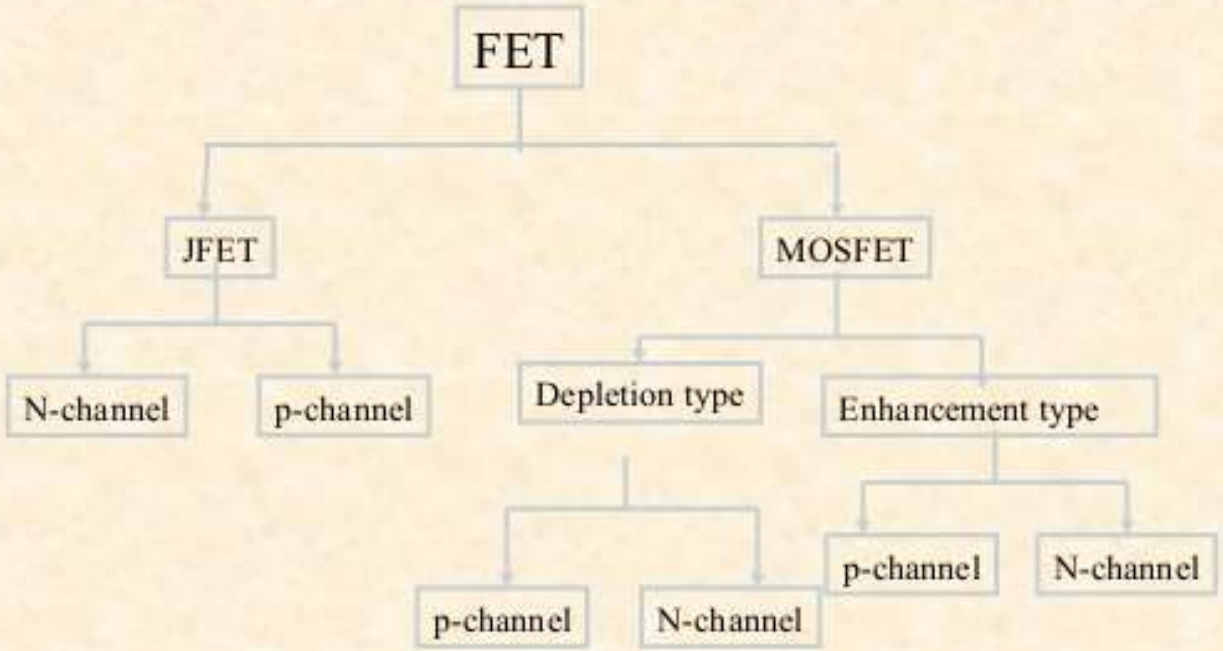
JFET Symbol

N Channel FET

P Channel FET

Fig 4 . JFET symbols

Classification of Field Effect Transistors



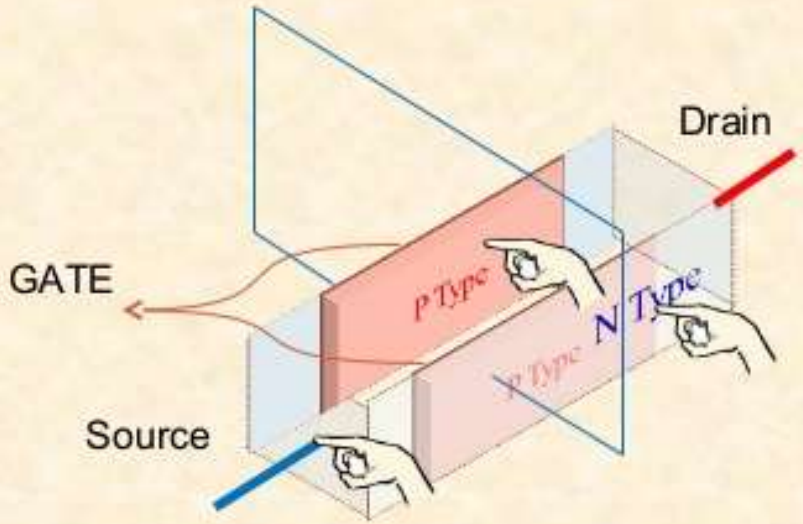
JFET

Based on the construction JFETS are of Two types

1.N Channel FET

2.P Channel FET

Construction



The two ends of the bar are known as Source and Drain

Fig 3. Construction of N Channel FET

Construction of FET

Source : The source is the terminal through which majority carriers enter the Silicon Bar

Drain : Terminal through which Majoroty carriers leave the bar

Gate: controls Drain current and is always reverse biased

Construction of FET

Analogy :

- The operation of FET can be compared to the water flow through a flexible pipe
- When One end is pressed the cross sectional area decreases hence water flow decreases
- In a FET drain is similar to outlet
- Gate is similar to control in the figure 2

Principle

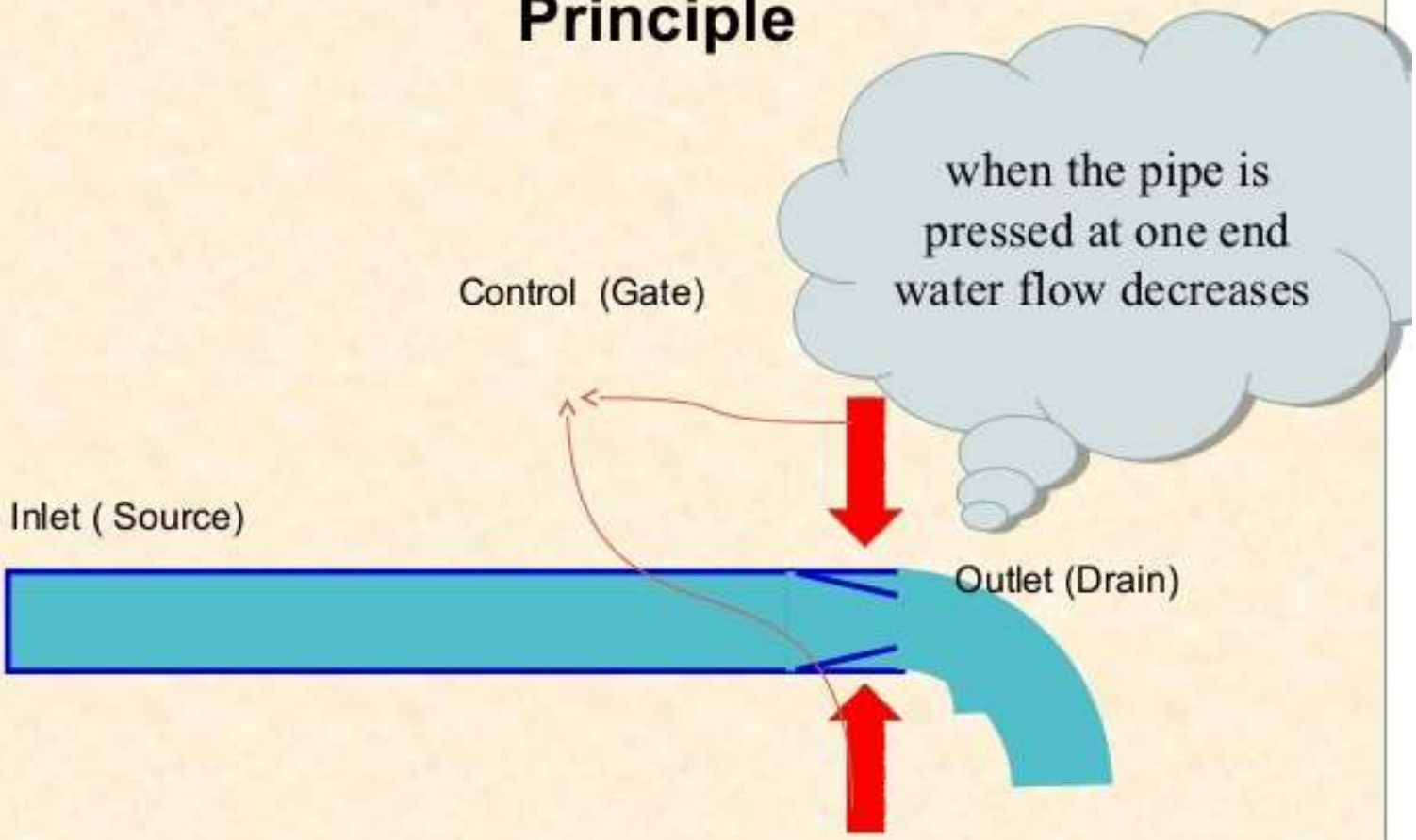


Fig2. water Pipe analogy

Operation

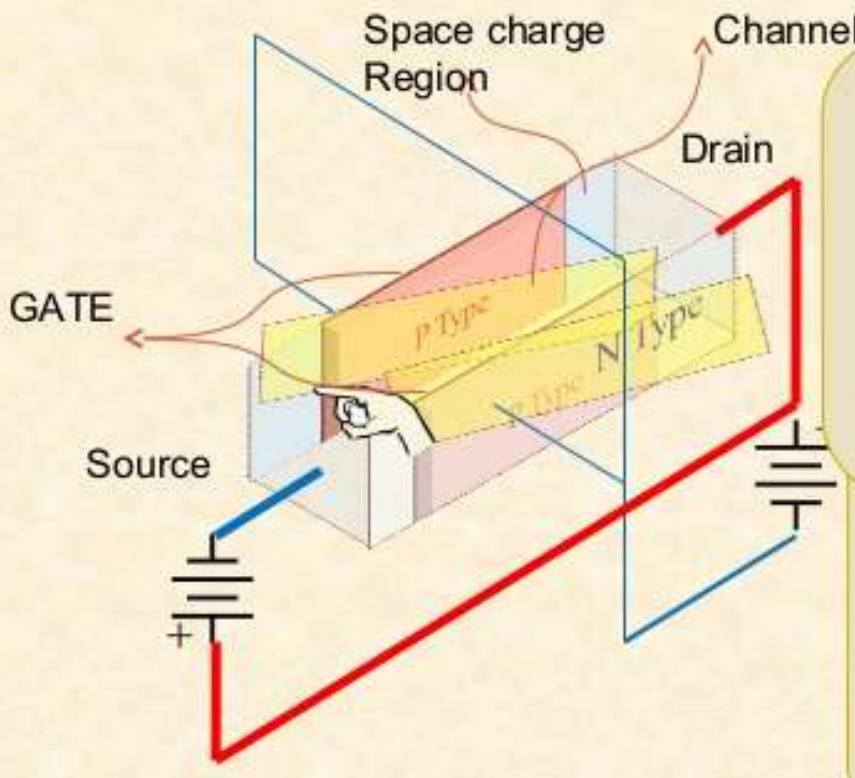
Principle : To control the drain current FET makes use of channel formed in by Space charge region between Gate and the bar

By increasing the reverse bias the width of space charge region decreases

As a result the channel Resistance increases

The Drain current decreases

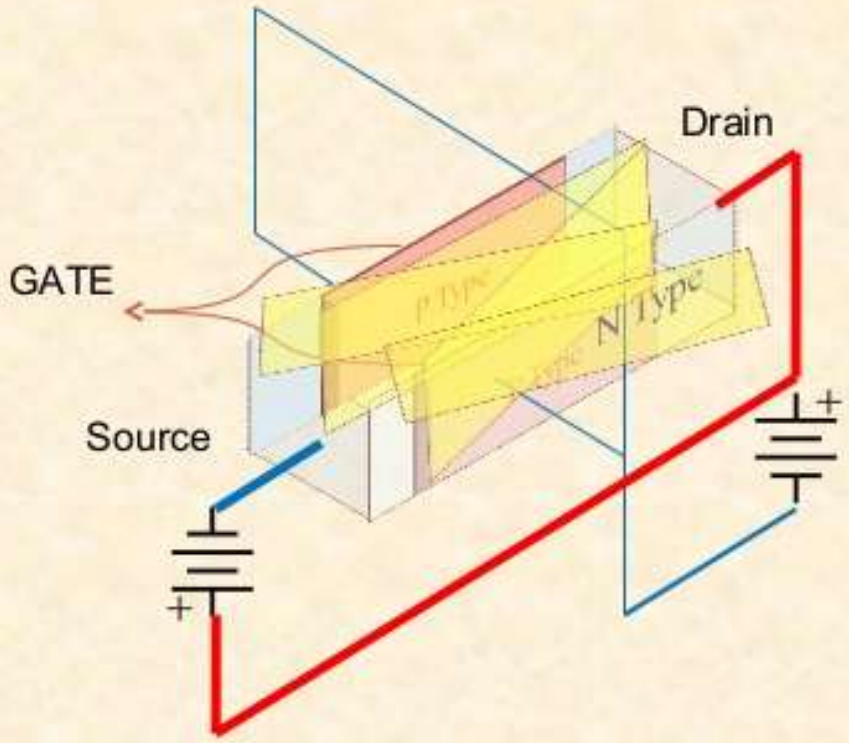
Working



As we increase the Reverse bias on Gate (V_{GS}) The channel width decreases

Gate is reverse Biased by battery 2

Working



The Bias voltage at which Drain current becomes Zero is Known as pinch off voltage

Working

N Channel FET	P Channel FET
Source connected to -VE	Source connected to +VE
Drain Connected to +ve	Drain Connected to -ve
Gate connected to –ve (Reverse Biased)	Gate connected to +ve (Reverse Biased)

Working

1. when Voltage is applied between source and Drain majority carriers move through the channel between depletion region
2. The value of Drain current is maximum when no external voltage is applied between gate and source
3. When gate to source reverse bias increases the depletion region widens and channel width decreases hence Drain current decreases

Working

1. Hence Drain current decreases
2. When gate to source voltage is increased further The channel completely closes
3. This is called pinch off region
4. This reduces Drain current to Zero
5. The Gate to source voltage at which the Drain current is zero is called " Pinch off Voltage"

P Type and N type FETs

N Channel FET	P Channel FET
1. Current carriers are Electrons	1.Current carriers are holes
2. Mobility of electrons is almost twice that of Holes in P channel FET	2.Mobility of holes is poor
3. Low input Noise	3.More noise
4. Large Transconductance	4.Low Transconductance

JFET Parameters

Electrical behavior is described in terms of the parameters of the Device. They are obtained from the characteristics. Important Parameters for FET are

1.DC Drain resistance

2.AC drain Resistance

3.Transconductance

JFET Parameters

1. DC Drain resistance : Defined as Ratio of Drain to source Voltage V_{DS} to Drain current $I_{D.}$ Also called static or Ohmic Resistance
2. Mathematically

$$R_{DS} = V_{DS}/I_D$$

JFET Parameters

1. AC Drain resistance : Defined as the resistance between Drain to source when JFET is operating in Pinch off Region or saturation Region
2. Mathematically

$$r_D = \frac{\Delta V_{DS}}{\Delta I_D}$$ When V_{GS} is constant

JFET Parameters

1. Transconductance (g_m): It is given by the ratio of small change in drain current to the corresponding change in the Gate to source Voltage VGS. Also known as Forward Transmittance
2. Mathematically

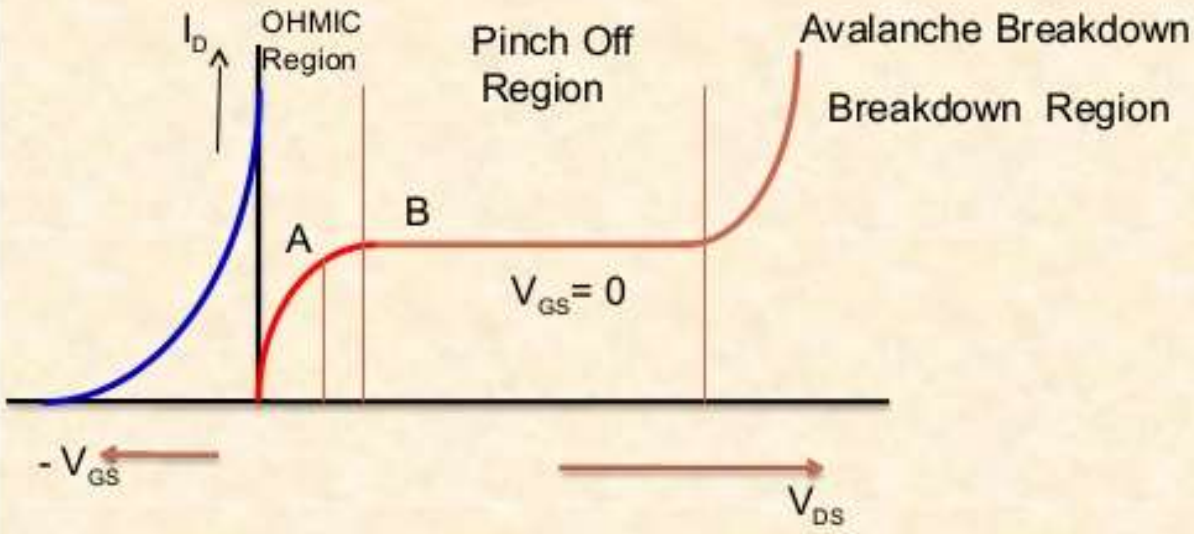
$$g_m = \frac{\Delta I_D}{\Delta V_{DS}}$$

FET and BJT

FET	BJT
1. Uni polar device	1. Bipolar device
2. Voltage controlled Device	2.Current controlled device
3. High input impedance (in Mega ohms)	3.Low input impedance
4. Better thermal stability	4.Low thermal stabilty
5. High switching speeds	5.Lower switching speeds
6. Less Noisy	6.More noisy
7. Easy to fabricate	7.Diffuicult to fabricate on IC

Drain Characteristics

Drain characteristics show the relation between the drain to source voltage and VDS and drain current ID



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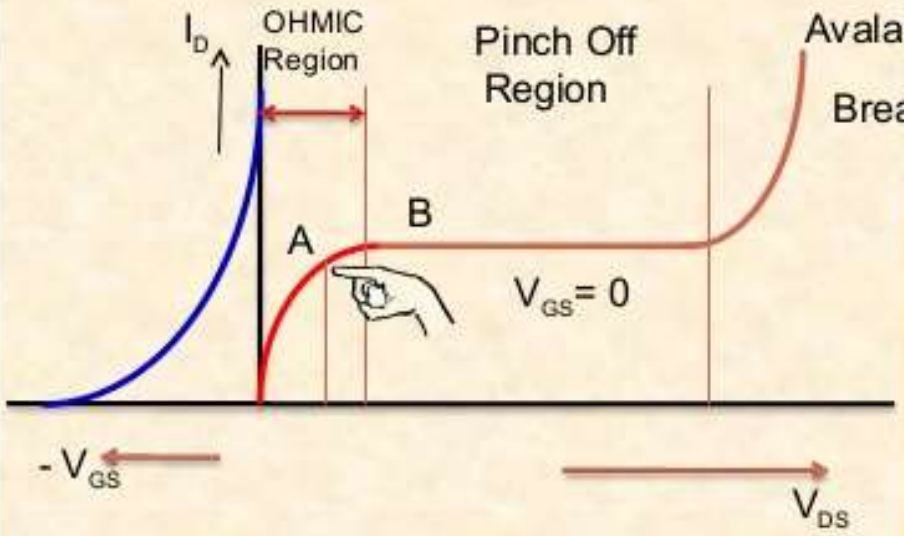
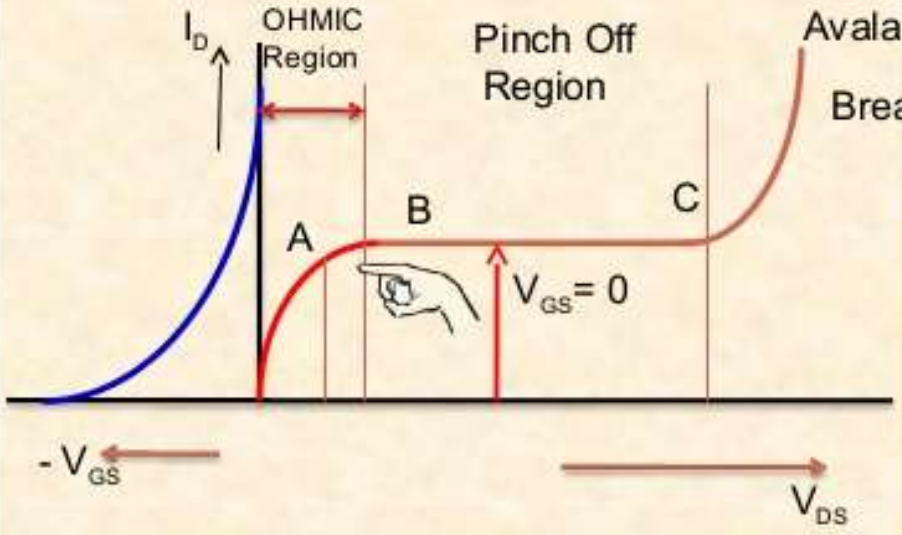


At the Drain to source Voltage corresponding to point B Channel width reduces to a minimum value and is known as pinch off

Drain Characteristics

Drain characteristics show the relation between the drain to source voltage and VDS and drain current ID

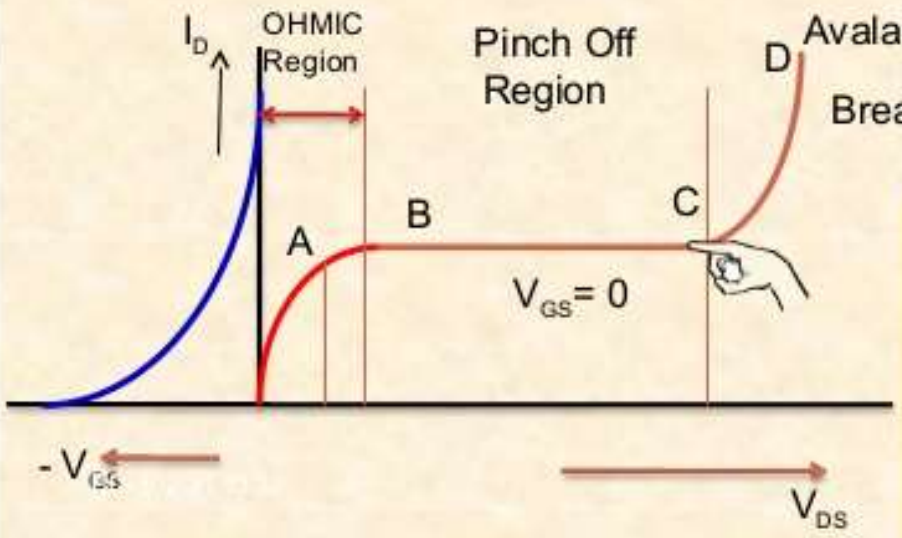


Drain current ID is given by

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Drain Characteristics

Drain characteristics show the relation between the drain to source voltage and VDS and drain current ID



The device gets damaged due to avalanche Breakdown mechanism

DISADVANTAGES OF FET OVER BJT

- FETs have a drawback of smaller gain bandwidth product compared to BJT.

Features

- The high input impedance, low output impedance and low noise level make FET for superior of the bipolar transistor.

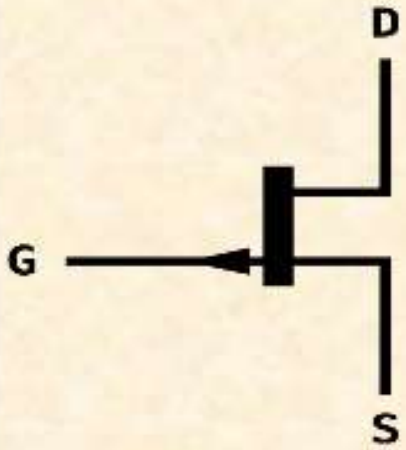
Applications

- As a buffer amplifier which isolates the preceding stage from the following stage.

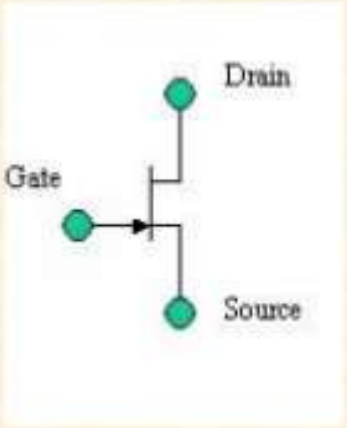
FET APPLICATIONS

Phase shift oscillators: The high input impedance of FET is especially valuable in phase shift oscillator to minimize the loading effect.

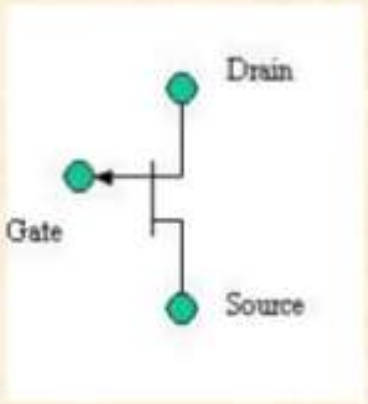
In voltmeters: The high input impedance of FET is useful in voltmeters to act as an input stage.



JFET



N CHANNEL JFET



P CHANNEL JFET